About RTL to GDSII Flow

SKYWater130 PDK

OpenLANE

Tools Used

AIM

Day 1 - Inception of open-source EDA, OpenLANE and Sky130 PDK

How to talk to computers

IC Terminologies

Introduction to RISC-V

RISC-V Characterstics

Software to Hardware

What happens when we run a program?

How does an application run on a computer?

SoC design and OpenLane

Introduction to Digital Design

What is a PDK?

Environment Setup

Simplified RTL to GDSII Flow

About OpenLANE

Getting familier to open-source EDA tools

Contents of the OpenLANE Directory

LAB Day 1

TASK 1: Finding the d flip flop ratio

Day 2 - Good floorplan vs bad floorplan and introduction to library cells

Chip Floor planning

Utilization factor and aspect ratio

Concept of pre-placed cells

De-coupling capacitors

Power planning

Pin Placement and logical cell placement blockage

Placement and routing

LAB Day 2

TASK 2: Calculating area

Day 3 - Design library cell using Magic Layout and ngspice characterization

LAB Day 3

Labs for CMOS inverter ngspice simulations